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(71) Applicant
Hughes Microelectronics
Limited
Fullerton Road
Glenrothes
Fife KY7 5PY
Scotland
(72) Inventor
Colin Walter Edwards
(74) Agents
Carpmaels & Ransford

(54) Non-volatile semiconductor memory cells

(57) Non-volatile bistable semiconductor latches having a pair of cross-coupled branches, each branch having a complementary driver or load and a driver connected in series at a respective node; at least one of the complementary drivers or loads, or drivers, includes a non-volatile IGFET having a variable threshold voltage (e.g. a FATMOS), said latch additionally including one or more buffer transistors (e.g. P-channel IGFETS) connected between one or both nodes and a latch output line. The buffer transistors increase the predictability of the state of the latch during power-up in a non-volatile mode of operation. Preferably the complementary drivers or loads, and the drivers, are constructed in CMOS or N-channel MOS. The buffers can drive a single DATA output line or twin DATA, $\overline{\text{DATA}}$ lines in a push-pull configuration.

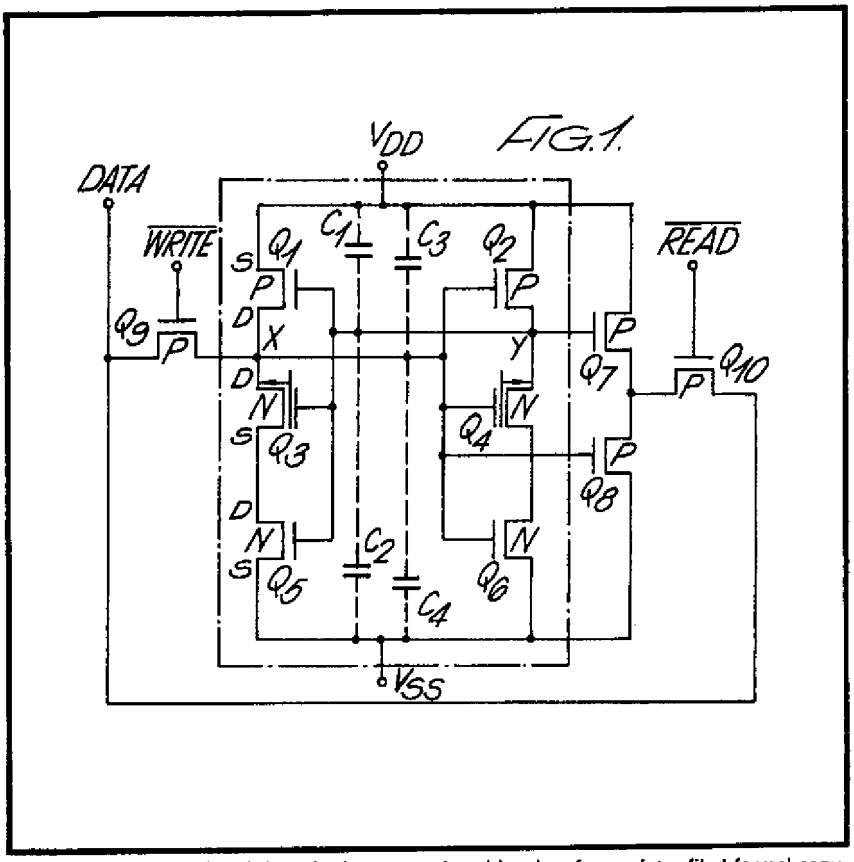
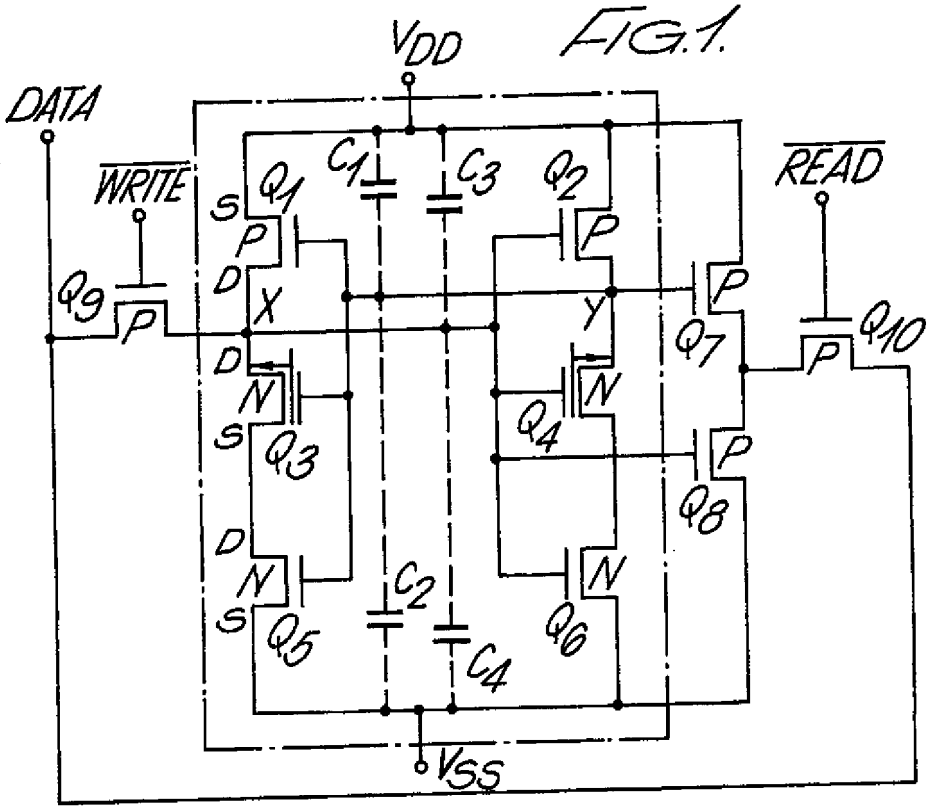


FIG.1.


VDD
DATA
WRITE
READ
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
C1
C2
C3
C4
P
N
S
D
X
Y
VSS

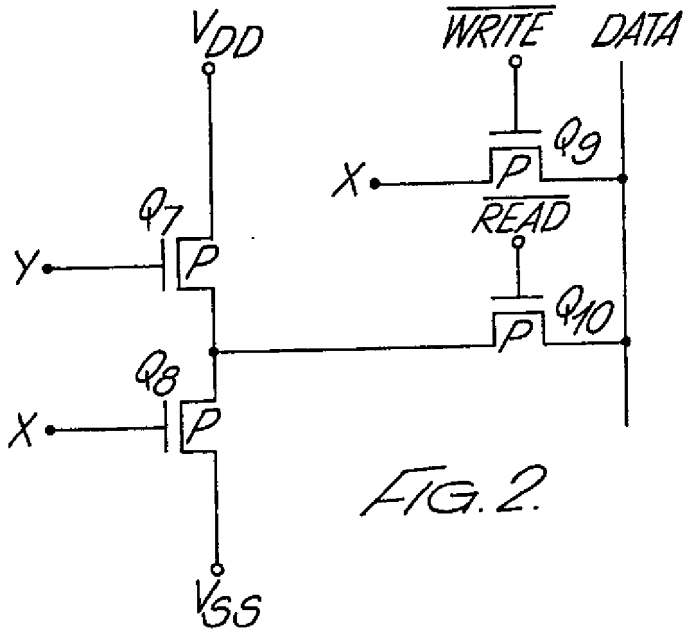
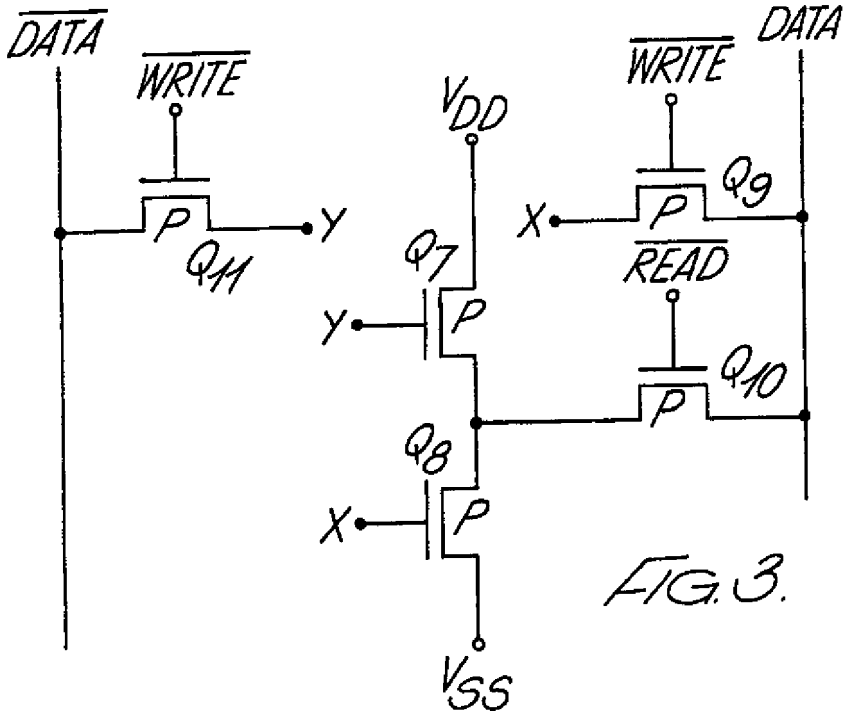

VDD
WRITE
DATA
Q9
X
READ
Q7
Y
Q10
Q8
X
VSS

FIG. 2.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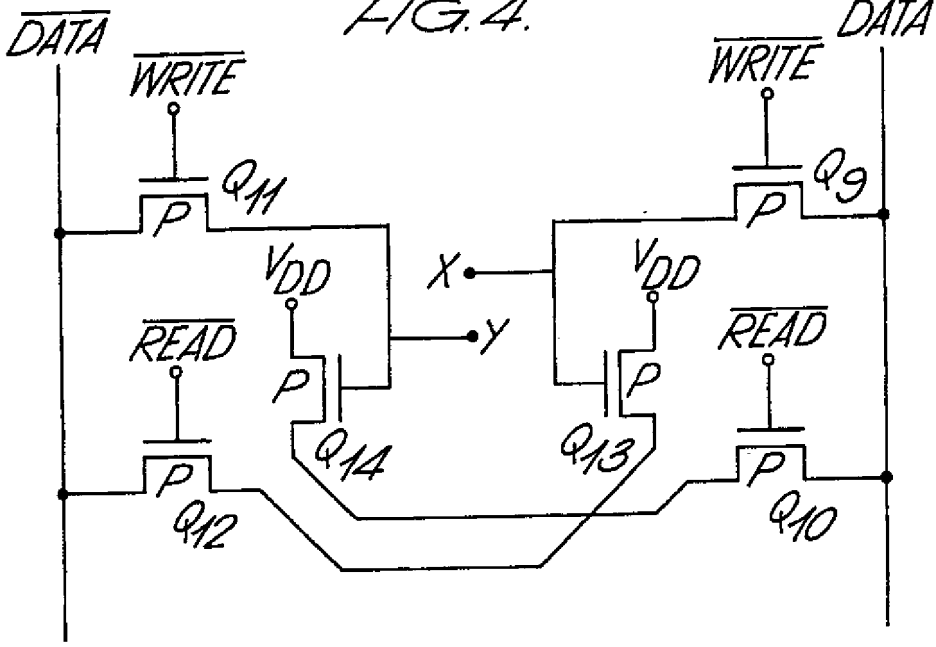
WRITE
P
Q11
Y
VDD
Q7
P
Y
Q8
P
X
VSS
WRITE
DATA
Q9
P
X
READ
Q10
P

FIG. 3.

FIG. 4.


DATA
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P
READ
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Q12
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X
VDD
P
Q13
WRITE
DATA
Q9
P
READ
P
Q10

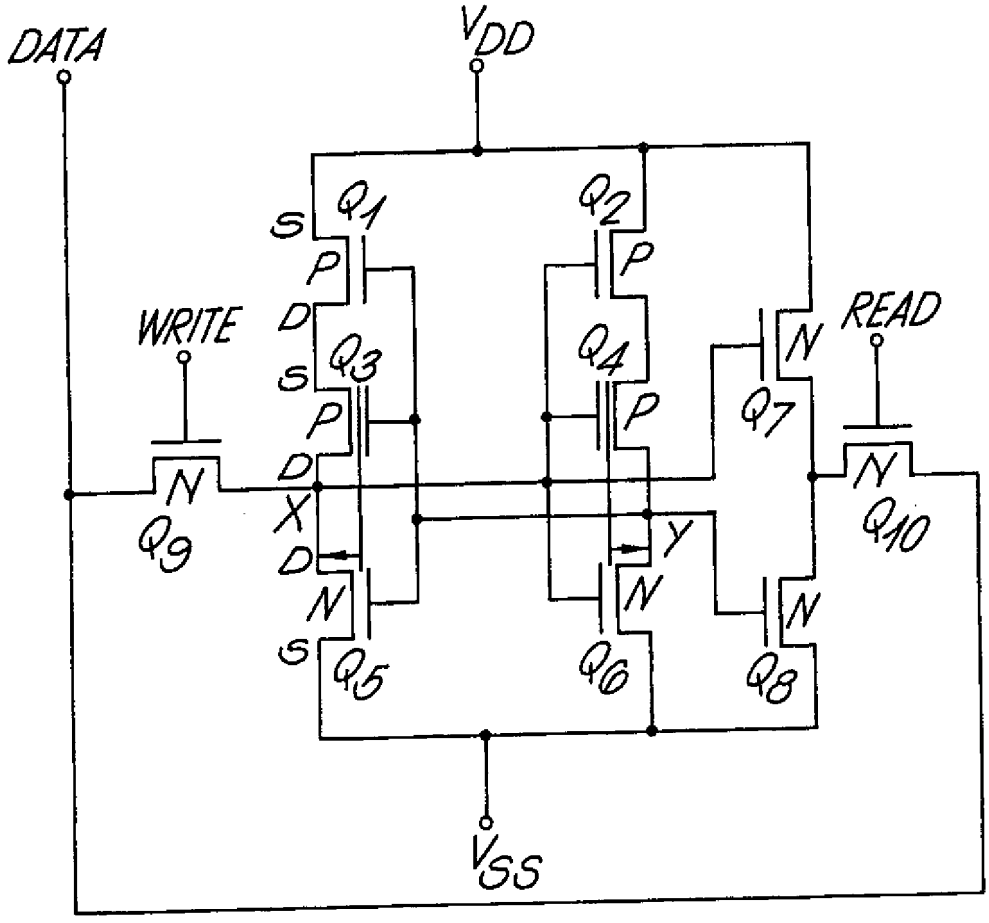

FIG. 5.

SPECIFICATION

Non-volatile semiconductor memory cells

This invention relates to semiconductor memory circuits which have the capability of retaining stored information even after electrical power to the circuit has been removed.

BACKGROUND OF THE INVENTION

Semiconductor memories can be classified as volatile (where stored information is lost upon power removal) and non-volatile (where stored information is maintained after power removal, and which can be accurately retrieved upon subsequent power-up). Several types of non-volatile semiconductor memories are known, notably based on MNOS transistors, FAMOS transistors, or FATMOS transistors. A description of prior MNOS and FAMOS memory circuits is given in U.S. Patent 4,132,904. The latter patent, together with U.K. Specification No. 2,000,407 describe and claim FATMOS non-volatile memory circuits.

The FATMOS is basically a control gate plus floating gate MOS transistor with a portion of the floating gate lying close to the semiconductor substrate. When the source and drain connections are connected to an appropriate potential (one positive relative to the other) and a suitable potential of a first magnitude applied to the control gate, the transistor conducts. Upon removal of the control gate potential, conduction ceases. If a potential of a second and higher magnitude is applied to the control gate with the drain at zero voltage, the transistor again conducts, but in addition electric charges tunnel between the floating gate and the transistor substrate through the portion of the floating gate closest to the substrate. This charge remains on the floating gate even when the control gate potential is removed and increases the switching threshold of the device. This charge on the floating gate enables the transistor to be employed in a non-volatile memory, as described in U.K. Specification No. 2,000,407. The non-volatility is removed by applying between the control gate and drain a potential of approximately the second and higher potential, but of opposite sign.

In a typical example of an N-channel enhancement-type FATMOS, the area of the floating gate closest to the substrate overlies the drain of the transistor. In normal, non-volatile operation, a voltage of typically + 5 to + 10 volts is applied to the control gate. To operate the device as a non-volatile transistor, a voltage of typically + 15 to + 25 volts is applied to the control gate.

Although FATMOS transistors work well when employed in non-volatile memory cells (see U.K. Specification No. 2,000,407) they can sometimes be unpredictable during power-up after the FATMOS's have been placed in their non-volatile mode. This unpredictability manifests itself by the FATMOS transistor(s) switching to the wrong state (i.e. a FATMOS with a charge retained on its floating gate being held "off" instead of "on", and vice-versa). The explanation for this appears to arise from the processing conditions employed to produce the N^+ diffusion areas. These have a higher capacitance per unit area than other semi-conductor areas, and the consequence is that the device has more nodal capacity to the negative supply line than the positive line. If, for example, one examines the CMOS non-volatile memory cell illustrated in Fig. 2a of U.S. Patent 4,132,904 (which employs a pair of FATMOS drivers in a cross-coupled latch configuration), the capacitance which exists between N1 and N2 to the more negative supply rail (V_{SS}) is greater than the corresponding capacitance to the more positive supply rail V_{DD}. Thus, when the cell is switched on after the FATMOS transistors (Q_2 and Q_4) have been placed in their non-volatile modes, the P-channel complementary driver or load transistors (Q_1 and Q_3) switch on faster than the FATMOS devices. They will thus make a decision regarding conduction states ahead of the FATMOS devices. The latter transistors may therefore possibly be driven into the incorrect states and are thus incapable of steering the latch into its correct, non-volatile memory state.

In addition to the above, it has also been found that when FATMOS devices are driven at high threshold (control gate) voltages, they become unpredictable as a consequence of their weaker driving capability.

The object of this invention is to improve FATMOS-containing non-volatile memory cells by increasing their reliability of action in their non-volatile modes.

SUMMARY OF THE INVENTION

The present invention reduces such unpredicatability as described by employing buffer transistors in each memory circuit, whereby to add capacitance between the cell nodes and the positive supply line. This enables the FATMOS devices to turn on first and thus enables them to dictate correctly the state to which the circuit should go. The buffers also remove the problem of unpredictable action in the FATMOS devices at high threshold levels by increasing the driving capability to the output (DATA) lines of the circuit.

According to the invention there is provided a non-volatile bistable semiconductor latch having a pair of cross-coupled branches connectable across a common supply voltage, each branch including a complementary driver or load and a driver connected in series at a respective node, at least one of said complementary drivers or loads, or drivers, including an insulated gate field effect transistor (IGFET)

having a variable threshold voltage whereby, when said threshold voltage is raised above a predetermined level, said transistor is rendered non-volatile to so render information held by the latch non-volatile, said latch additionally including one or more buffer transistors connected between one or both nodes and an output line of the latch.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred features of the invention will now be described, with reference to the accompanying drawings, given by way of example, wherein:–

Figures 1 and 2 are electrical circuit diagrams of a first embodiment of the invention;

Figures 3 and 4 are circuit diagrams of second and third embodiments of the invention, respectively;

Figure 5 is a circuit diagram of a fourth embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A first embodiment of the invention is illustrated in Figs. 1 and 2.

Referring to Fig. 1, there is illustrated a CMOS NOVRAM latch having P-channel complementary drivers (or loads) Q_1, Q_2 and N-channel drivers constituted by FATMOS devices Q_3, Q_4 and MOS transistors Q_5, Q_6. The control gates of the transistors are cross-coupled to the nodes of each opposite branch of the cell, such nodes being indicated as X and Y. The notional capacitances between the nodes and the supply rails V_{DD}, V_{SS} are indicated by dashed lines and capacitors C_1 to C_4. As so far described the cell (when coupled to N-channel READ and WRITE transistors) is identical to that illustrated in Fig. 6 of U.K. Specification No. 2,000,407, and thus a detailed description of its volatile and non-volatile operational states will not be given here—the reader being referred to said U.K. Specification for details.

Before describing the inventive aspects shown in Figs. 1 and 2, the unpredictability of the circuit will first be explained, reference being made to that part of latch within the dotted-dashed box of Fig. 1. At power-up, in a non-volatile mode of operation, one of the FATMOS devices Q_3, Q_4 will be off and the other on as a consequence of the charge stored on the floating gate of the "on" one of the two devices. This characteristic should therefore force the latch into an unambiguous memory state which has been set previously by placing the FATMOS devices into the non-volatile conditions described. However, as has already been explained, the N^+ diffusion areas have a high capacitance per unit area and thus $C_2 > C_1$ and $C_4 > C_3$. When power is applied to the cell, the P transistors Q_1 and Q_2 turn on faster than Q_3 to Q_6 and can themselves set the state of the latch ahead of conduction by the FATMOS devices. The memory state of the latch is hence dictated by the (unpredictable) states in which Q_1 and Q_2 settle, and not by the states predicted by the non-volatile charges on the FATMOS devices.

Reverting now to the full illustration in Fig. 1, this unpredictability is removed by adding P-channel buffer transistors Q_7, Q_8 between the DATA READ line and the nodes X and Y. In this manner, the control gate of Q_7 essentially increases the capacitance C_1 and the control gate of Q_8 increases the capacitance C_3. Ideally, the dimensions and characteristics of Q_7 and Q_8 are selected so that $C_1 >> C_2$ and $C_3 >> C_4$. Under such a circumstance the N-channel drivers Q_3 to Q_6 turn on before the P-channel devices Q_1 and Q_2 during power-up and thus the memory state of the cell is correctly and predictably determined by the non-volatile states of the FATMOS devices Q_3 and Q_4. The addition of the buffers also increases the driving capability of the latch and reduces the likelihood of unpredictable action when the FATMOS devices are operated at very high threshold voltages. The WRITE and READ transistors (Q_9 and Q_{10} respectively) which couple the latch to a DATA line are also P-channel devices and are activated by negative potentials ($\overline{\text{WRITE}}$ and $\overline{\text{READ}}$) applied to their gates. By making these latter transistors as P-channel devices, they serve to further increase the capacitances C_1 and C_3 and ensure that $C_1 >> C_2$, $C_3 >> C_4$.

The circuit shown in Fig. 1 is shown in simplified form in Fig. 2, where the latch components have been omitted but with the coupling points to the latch nodes, X, Y shown.

The embodiment described in Figs. 1 and 2 receives its input and provides its output through a single DATA line, but this is not essential. Alternative embodiments are illustrated in Figs. 3 and 4.

In Fig. 3, a push-pull WRITE input is shown from DATA and $\overline{\text{DATA}}$ lines. An additional P-channel transistor Q_{11} provides the input to node Y from a $\overline{\text{DATA}}$ line.

In Fig. 4, a fully symmetrical, latch is shown. This has push-pull WRITE input and READ output to and from both nodes. An additional P-channel transistor Q_{12} provides the READ output to the $\overline{\text{DATA}}$ line. The buffer transistors Q_7 and Q_8 of Figs. 1 to 3 are configured slightly differently and are shown as Q_{13} and Q_{14}, linking the X and Y nodes to the Q_{10} and Q_{12} READ transistors respectively. In order to enable this circuit to function adequately, the DATA and $\overline{\text{DATA}}$ lines are precharged before reading of the latch takes place. The technique of precharging data lines of RAM cells is well-known.

A further embodiment of the invention is illustrated in Fig. 5. This embodiment is a CMOS NOVRAM latch similar to that illustrated in Figs. 1 and 2 except that P-channel

rather than N-channel FATMOS devices Q_3, Q_4 are employed. The tunnels of Q_3 and Q_4 extend between their floating gates and the N^+ regions of the drains of the adjacent transistors Q_5 and Q_6 respectively. The gates of the buffer transistors Q_7 and Q_8 respectively. The gates of the buffer transistors Q_7 and Q_8 (N-channel devices) are connected to the opposite nodes (X, Y) shown in Fig. 1 and, also, the read and write transistors Q_9 and Q_{10} are N-channel devices.

It will be appreciated that the Fig. 5 embodiment may be further modified to include a push-pull write operation (similar to that shown in Fig. 3) or a fully-symmetrical operation (similar to that shown in Fig. 4) with appropriate substitution of N-channel for P-channel read and write transistors and reversal of node coupling to the buffer transistors where necessary.

Several further alternative circuit arrangements in accordance with the invention are possible. For example, the buffer transistors may be employed to advantage in the fully N–MOS latch illustrated in Figs. 8 or 9 of U.K. Specification No. 2,000,407. The N–MOS transistors Q_5, Q_6 in series with the FATMOS drivers may be omitted if desired (e.g. see the circuit of Fig. 1a of U.K. Specification No. 2,000,407). Moreover, one or other of the FATMOS devices may be omitted or made to form the complementary driver(s) rather than the drivers themselves (see Figs. 1b, 7, or 15 to 21 in U.K. Specification No. 2,000,407). The complementary driver transistors Q_1, Q_2 may be replaced by resistive loads if desired (see Fig. 10 of U.K. Specification No. 2,000,407).

CLAIMS

1. A non-volatile bistable semiconductor latch having a pair of cross-coupled branches connectable across a common supply voltage, each branch including a complementary driver or load and a driver connected in series at a respective node, at least one of said complementary drivers or loads, or drivers, including an insulated gate field effect transistor (IGFET) having a variable threshold voltage whereby, when said threshold voltage is raised above a predetermined level, said transistor is rendered non-volatile to so render information held by the latch non-volatile, said latch additionally including one or more buffer transistors connected between one or both nodes and an output line of the latch.

2. A latch according to claim 1 wherein said complementary drivers or loads and said drivers are IGFETS.

3. A latch according to claim 2 wherein either each of said complementary drivers or loads or each of said drivers includes a respective one of said IGFETS having said variable threshold voltage.

4. A latch according to any of claims 1 to 3, wherein each node is connected to the control gate of a respective IGFET P-channel buffer transistor having its source to drain circuit in series with an output line of the latch.

5. A latch according to claim 4 comprising a pair of said IGFET P-channel buffer transistors having their source to drain circuits in series for connection across a common voltage supply, the junction between said buffer transistors being connected to a DATA output line of the latch.

6. A latch according to claim 4 comprising a pair of said IGFET P-channel buffer transistors, one having its source to drain circuit connected in series with a DATA output line of the latch and the other having its source to drain circuit connected in series with a DATA output line of the latch.

7. A latch according to any of claims 1 to 6, wherein said complementary drivers or loads, and said drivers are constituted in CMOS circuitry.

8. A latch according to any of claims 1 to 7, wherein said complementary drivers or loads, and said drivers are all constituted in N-channel MOS circuitry.

9. A non-volatile bistable semiconductor latch substantially as herein described with reference to Figs. 1 and 2, or 3 or 4 or 5 of the accompanying drawings.

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